REMARKS

Claims 1-2 have been canceled. Claims 3, 5, and 6-7 are currently amended. Applicant contends that the amendments are fully supported by the Specification as originally filed and thus do not introduce new matter.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-2, 5-8 were rejected under 35 U.S.C. § 102(b) as being anticipated by Tang et al. (U.S. Patent No. 6,172,915). Applicant respectfully submits that the present application has an effective filing date of March 9, 2001, which is less than one year after the issue date of Tang et al. Specifically, as indicated in paragraph [0001] of the present application, the present application is a divisional of United States Patent Application Serial No. 10/265,560 filed October 7, 2002 and titled, "NON-VOLATILE MEMORY DEVICE WITH ERASE ADDRESS REGISTER," which is a Divisional of Serial No. 09/802,612 filed March 9, 2001 and titled, "NON-VOLATILE MEMORY DEVICE WITH ERASE ADDRESS REGISTER." Therefore, Applicant respectfully submits that Tang et al. qualifies as a reference under 35 U.S.C. § 102(e). Applicant respectfully traverses.

Claims 1-2 have been canceled, thus overcoming the rejection thereto.

Claim 3, as currently amended, includes all of the limitations of the base claim (claim 1) and any intervening claims (claim 2). As indicated below, the Examiner indicated that claim 3 would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. Therefore claim 3 should be allowed.

Claim 5, as currently amended, depends directly from claim 3 and thus includes patentable limitations of claim 3. Therefore, claim 5 should be allowed.

Claims 6 and 8, as currently amended, each include an address counter coupled to an address register corresponding to memory sub-blocks; and control circuitry coupled to a plurality of blocks of memory each having groups of the memory sub-blocks, the control circuitry capable of executing an erase verification operation, the operation comprising selecting an addressable block of memory cells, identifying an address of a memory cell in the addressable block by reading contents of the address register, wherein the address is greater than a lowest address in

the selected addressable block, copying the contents of the address register to an address counter, and performing an erase verification of the memory cell.

Applicant finds no indication or suggestion in Tang et al. of an address counter coupled to an address register corresponding to memory sub-blocks or control circuitry capable of copying the contents of the address register to an address counter, as in each of claims 6 and 8. Therefore, Tang et al. does not include each and every element of claim 6 or 8, so claims 6 and 8 should be allowed.

Claim 7 depends directly from claim 6 and thus includes patentable limitations of claim 6. Therefore, claim 7 should be allowed.

Allowable Subject Matter

Claims 3-4 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. Applicant thanks the Examiner for this indication. Claim 3, as currently amended, includes all of the limitations of the base claim (claim 1) and any intervening claims (claim 2), and should be allowable.

Claim 4 has not been rewritten. Claim 4 depends directly from claim 3 and thus includes patentable limitations of claim 3. Therefore, claim 4 should be allowed.

CONCLUSION

Applicant believes that the claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. The Examiner is invited to contact Applicant's Representative at direct dial (612) 312-2208 if there are any questions regarding this Response or if prosecution of this application may be assisted thereby.

Respectfully submitted,

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